Designing For Space And High Reliability Environments

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A Comparison of Space-Grade FPGAs

The capability of space-grade FPGAs has improved significantly since the launch of six Actel A1020-CQ84Bs on-board NASA's, Sampex spacecraft in 1992. The A1020 was fabricated on a 2 µm process, contained 547 logic cells each comprising a 4:1 MUX and an OR gate.

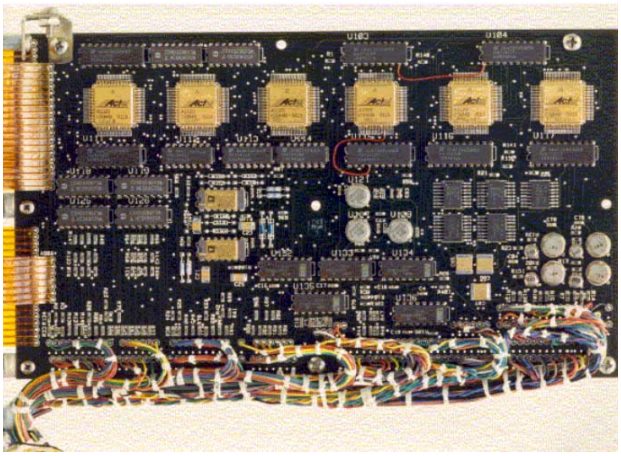


Figure 1: The Actel A1020-CQ84B FPGAs used within Sampex's data processing unit.

FPGAs are increasingly being used in almost every spacecraft sub-system and designers now have a choice of fabrics and different technologies. Which one is right for your mission?

The latest devices are manufactured using deep, submicron technologies offering thousands of logic cells, almost 1000 I/O, high-speed serial links, CPUs, dedicated DSP processors, as well as re-usable IP cores. Space-grade FPGAs are offered in three major process technologies: SRAM, flash and antifuse.

SRAM-based FPGAs are volatile and need to be re-programmed at each power-up. This eases prototyping and allows devices to be completely re-configured in-orbit. SRAM configuration memory can be sensitive to radiation effects which can potentially corrupt a design and alter the intended operation. Some space-grade devices use the standard, un-hardened, 6-transistor, storage cell in the functional logic blocks, while more SEU-robust parts exploit the radiation tolerance advantages of a 12-transistor design at the expense of increased area and power consumption. Continued CMOS scaling has helped to alleviate these disadvantages somewhat.

Flash-based FPGAs are non-volatile, live at power-up, and can be re-programmed in-orbit. A floating-gate transistor is used within each cell which is immune to firm errors as exposure to radiation cannot generate sufficient charge to change its configuration state. Flash memory cells typically require two transistors resulting in increased logic density, shorter routing, smaller interconnect delays and lower power consumption compared to SRAM devices.

Antifuse-based FPGAs are non-volatile, live at power-up, but one-time programmable, which can present prototyping challenges. The antifuses which configure the interconnect are grown between the upper two layers of metal eliminating the routing channels and switching resources between logic

modules. This results in increased logic density, shorter routing and smaller delays. Antifuse FPGAs also consume less static and dynamic power than equivalent SRAM devices.

Flash and antifuse FPGAs require additional processing steps compared to bulk CMOS which has resulted in the specifications of these devices lagging SRAM-based parts by several generations. The increased capacity, the diversity of the resources, faster operation and lower dynamic power offered by deep-submicron, SRAM-based devices can offset the intrinsic energy consumption and logic density advantages of flash and antifuse parts.

Smaller geometries have resulted in less dynamic power consumption because of lower core voltages and smaller gate capacitances. However, ultra deep-submicron processes dissipate more static energy because of increased leakage and subthreshold currents.

CMOS scaling has improved the total-dose and latch-up sensitivity of space-grade microelectronics. Thinner gate oxides trap less positive charge while lower supply voltages and the reduced gain of the parasitic, bipolar, silicon-controlled rectifier bolster total-dose and latch-up immunity respectively. SEE mitigation has become more challenging as increased logic densities require less overall charge to disrupt sensitive locations.

Some space-grade FPGAs have been hardened-by-process, fabricated using a CMOS silicon-on-insulator process, or use an epitaxial layer to protect against radiation-induced latch-up.

Other space-grade FPGAs contain intrinsic architectural and circuit-level features to protect against upsets and transients at the expense of area, power consumption and performance. The flip-flops within antifuse FPGAs are typically triplicated and upsets due to single ion strikes are voted out by the unaffected latches. The latest flash parts contain SET filters to suppress transients generated with combinatorial logic. One supplier of SRAM-based devices has replaced the standard, 6-transistor, functional element with a radiation-hardened, 12-transistor design shown below. In the conventional cell, a particle striking node Q may cause the latch to change state resulting in an SEE. In the hardened version, Q is represented at two different nodes and a strike at either cannot cause an upset. The number of transistors per latch has doubled, which can significantly reduce the available gate count in a given circuit area.

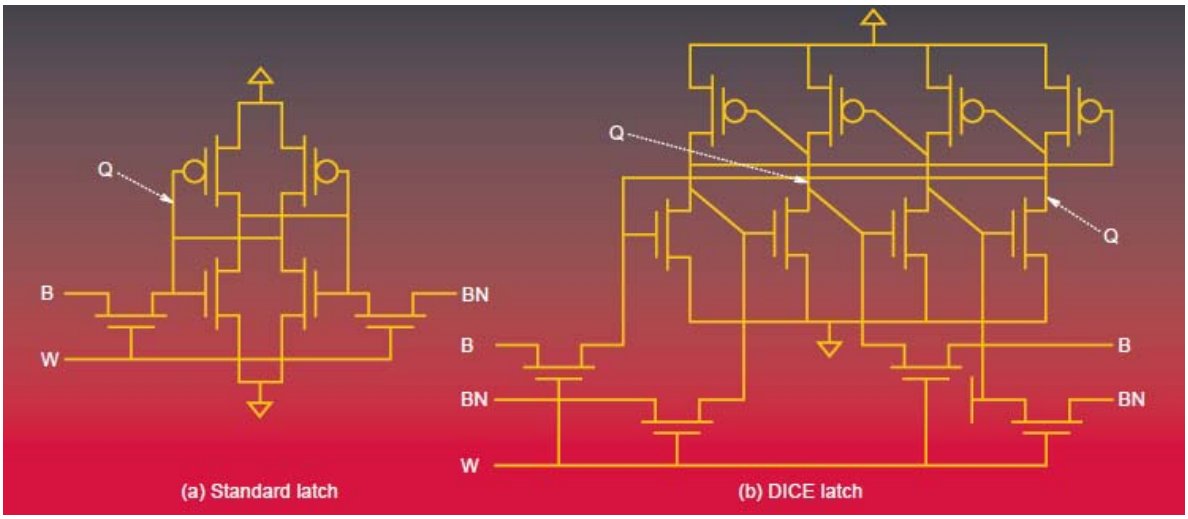


Figure 2: Standard and radiation-hardened SRAM storage cells.

Block RAM and configuration memory contain error detection and correction to protect against SEUs. To reduce the effects of multi-bit errors, some vendors have interleaved the layout of configuration memory such that physically adjacent errors are separated in the memory map. This makes errors appear as separate single-bit upsets enabling them to be repaired. Not all configuration memory is critical to FPGA operation and several suppliers allow users to define hierarchical regions in the design and partition this into essential and non-essential bits. Soft-error detection and correction focuses on those bits necessary for logic design and techniques such as scrubbing and partial configuration can be used to prevent the accumulation of configuration errors due to SEEs.

Some manufacturers provide proprietary tools that automatically triplicate registers, combinational logic, voters, global buffers and I/O to protect against SEUs and SETs. State machines can be protected against SEEs by choosing fault-tolerant coding schemes and third-party EDA vendors also provide software which adds triple-mode redundancy to the HDL or during synthesis, *e.g.* Mentor Graphics' Precision.

It's important to note that FPGA SEE mitigation techniques do not prevent upsets nor transients, but allow designs to get through periods of error detection and correction without interruption, thereby reducing the effective FIT rate and increasing design availability.

The following table lists the devices that were compared for this article:

FPGA #	Technology	Node (nm)	Power (mW)
1	SRAM	90	960
2	Flash	130	12
3	Antifuse	250	125
4	SRAM	180	780
5	SRAM	28	1036
6	SRAM	65	5400
7	Antifuse	150	270

8	Flash	130	7.2
9	Flash	65	142
10	Antifuse	150	87
11	SRAM	150	780
12	SRAM	90	482
13	SRAM	28	915

Table 1: Candidate Space-Grade FPGAs

For obvious reasons and to maintain my independence, I will not reveal the identity of the FPGAs compared in this article. Most of the devices comprise LUT-based, logic elements, with several having MUX-based, configurable fabric. Other FPGAs have flown or are scheduled to be launched, but this comparison has been restricted to devices that are or will formally become space-qualified.

This article compares the predicted, average, power consumption following synthesis and place & route, accounting for different process technologies, diverse fabric types, FPGA size, logic density, the impact of CMOS scaling and hardening.

I coded VHDL of a maximal-length, 20-stage, many-to-one LFSR: for each FPGA, this design was synthesised to map the RTL to the target primitives, followed by placement, routing and post-layout functional verification. Conceptually, the gate-level netlist comprises 20 registers, one two-input XOR gate and 21 primary I/O.

For this initial comparison, I deliberately did not specify any stringent constraints for logic synthesis nor did I optimise the standard floorplan of the placed design. Shift-register macros or proprietary IP cores were not considered either!

A clock frequency of 50 MHz was used and a maximum toggle rate was assumed for the maximal-length LFSR. The ultra deep-submicron devices can operate at much higher frequency but the slowest FPGA considered in this comparison is limited to 50 MHz. Table 1 lists the predicted, average, power dissipation for all parts: for many of the devices, the energy consumed by the core to implement this simple LFSR was negligible, dominated mostly by I/O as well as some static leakage.

FPGA vendors offer different tools to predict power consumption: some provide spreadsheets that estimate dissipation during the project concept phase based on an initial assessment of the logic resources required, I/O loading and activity rates. This information can be entered manually or extracted from the gate-level netlist output by the synthesis tool. The estimate for FPGA 9 was obtained from a pre-synthesis spreadsheet.

Several suppliers offer more accurate predictions following place and route using design-activity information generated during simulation (VCD/IEEE 1364 file). Analyses software is available that reports junction temperature as well as average and cycle-accurate, peak static and dynamic power consumption at gate, net, cell, I/O, clock domain and resource level. This more detailed breakdown has proved to be invaluable on projects!

It's important to note that the ultra deep-submicron, SRAM-based FPGAs listed above contain many hundreds of thousands of configurable logic elements. At these geometries, static power has much more impact on overall consumption and power-driven synthesis can be used to lower dissipation. The variation in the predicted energy and the division between dynamic and static consumption due to the combined effects of different process technologies, diverse fabric types, FPGA size, logic density, the impact of CMOS scaling and hardening is very insightful.

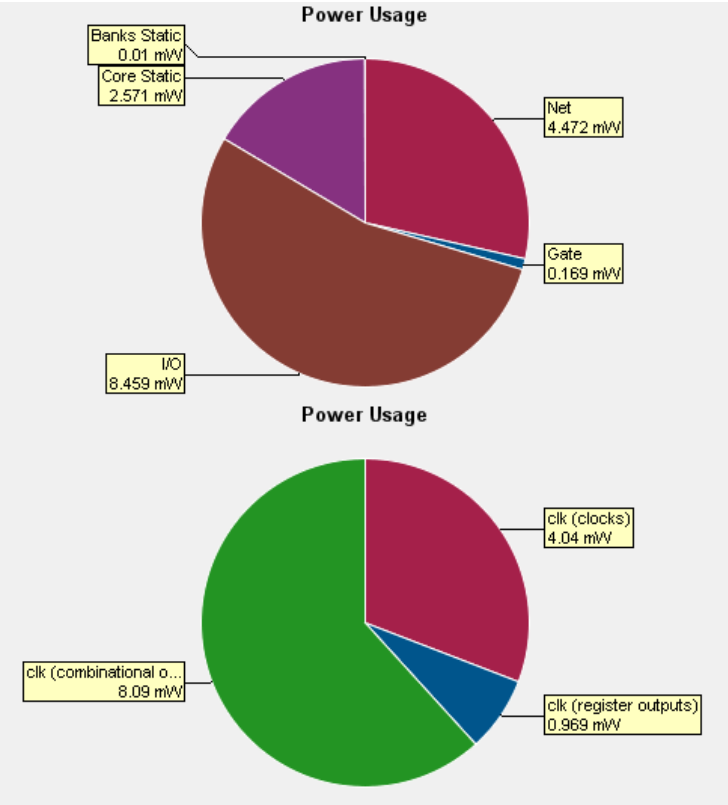


Figure 3: Predicted, average, power-consumption breakdown.

In the absence of real hardware, comparing power-consumption predictions between FPGAs can be like equating 'apples to oranges'. The various suppliers offer different levels and accuracies of estimating dissipation and some do not differentiate between static and dynamic power.

Not every spacecraft requires the latest, deep-submicron, 1 GHz, 1700-pin FPGA with many sub-system baselining smaller, 200-pin devices clocking at 50 MHz. However, only the former can meet the processing throughputs required by a telecommunication payload while the latter can be used to provide localised digital control.

When selecting a space-grade FPGA, there will be many, program-specific requirements, *e.g.* are there sufficient logic resources to meet the mission's processing needs, unit cost, legacy of use, the suitability of the package, its size and pin pitch, ease of assembly onto a PCB and the qualification of the mounting to withstand shock and vibration, prototyping options, the number of supply rails, the design of the

power-distribution architecture and its efficiency, the number and type of I/O and the configuration architecture. Operational considerations including the required reliability and the radiation environment specific to the mission will also influence the choice of FPGA.

Today, architecting space-grade hardware adopts a more systems-based approach to ensure designs are developed to cost and schedule, are scalable, and re-usable for multiple mission types. The latest FPGAs are large and complex, and careful selection of companion components is necessary to ensure systems are right-first-time. As an example, the use of high-efficiency, DC-DC convertors that generate multiple, isolated, regulated, supply rails directly from the spacecraft bus, to power an FPGA simultaneously switching many hundreds of I/O to minimise coupling and the generation of unwanted EMI. The use of on-chip and off-chip, design-for-EMC techniques and circuit simulation is mandatory to deliver the requested system performance to customers.

Conclusion

FPGAs are increasingly being used in almost every spacecraft sub-system and designers now have a choice of fabrics and different technologies. This article compared the predicted, average, power consumption for a 20-stage, many-to-one LFSR implemented on the range of space-grade FPGAs, accounting for different technologies, geometries, FPGA size, logic density, the impact of CMOS scaling and hardening.

Different mission types use FPGAs in diverse ways, *e.g.* a LEO Earth-observation payload that operates for five minutes out of every ninety in a polar orbit has unique requirements compared to an FPGA which has to function continuously for up to eighteen years on-board a GEO telecommunication satellite.

Further comparisons of the space-grade FPGAs listed in this article can be viewed on my blog, **Out-of-this-World-Design**, at http://www.edn.com/electronics-blogs/4406636/Out-of-this-World-Design.

Author Biography

Dr. Rajan Bedi has been leading the design and development of space electronics at Astrium Ltd. (now Airbus) for twelve years. Rajan partners with the world's leading electronics and test companies to advance their capability together with the space industry, producing some of the most enabling semiconductors and technologies currently in-orbit. As Head of the Mixed-Signal Design Group, Rajan's team led the R&D and hardware development of the award-winning, channelizing payload currently operating on-board the Alphasat telecommunication satellite.

Each month Rajan publishes an article on his blog, **Out-of-this-World Design**, and welcomes feedback: http://www.edn.com/electronics-blogs/4406636/Out-of-this-World-Design

Experior Raises the Bar for Vibration and Shock Testing

Checkout these demanding test levels that Experior Labs can now perform routinely using its high performance Unholtz-Dickie T2000 Shakers. The specific test levels listed below are all based on a total payload weight of 25 lbs added to the armature.

Test Type	Max Test Level
Random Vibration (20 Hz - 2,000 Hz) ……	155 G rms
Sine Sweep Vibration (up to 2,000 Hz) ……	185 G pk
Classical Shock Pulse (Halfsine or Sawtooth) ……....	500 G pk
SRS Shaker Shock (100 Hz – 10 KHz) …… Q = 10	3,500 G (SRS)

The key to achieving these extreme g-levels is the Model T2000 Shaker and its solid metal, inductively coupled armature. This unique **Induct-A-Ring armature** weighs only 110 lbs and can generate up to 25,000 lbs pk sine / 23,000 lbs rms random and 67,000 lbs pk shock force.

The data screens below illustrate a variety of actual tests conducted recently at Experior Labs in Oxnard, CA.

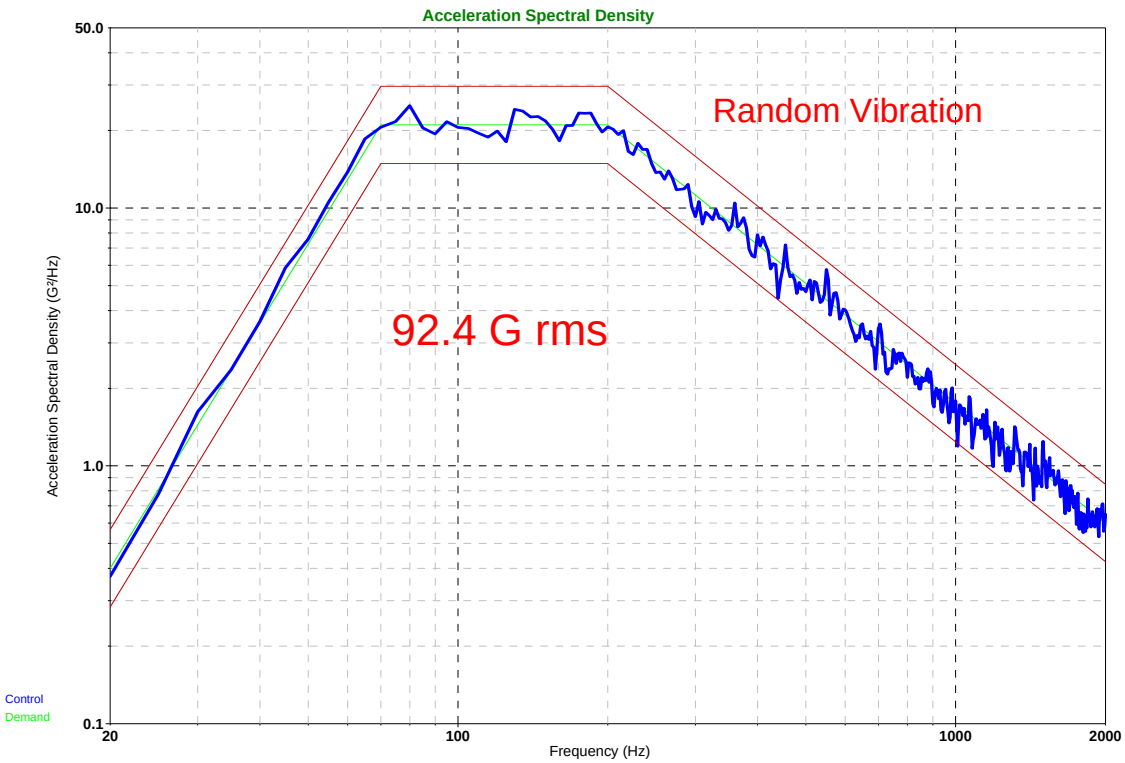


Fig 1: Random PSD @ 92.4 G rms with 21.0 g^2/Hz in mid-band

The random vibration associated with a rocket launch is a brutal dynamic environment that often calls for highly shaped PSD profiles as seen in Figure 1. The shaped PSD profile shown here has a major concentration of g2/Hz energy in a part of the test spectrum where the electrodynamic shaker armature has a significant percentage of "resistive" impedance, which means that output current and voltage from the Power Amplifier in this resistive band must be "in-phase" – this in turn produces high heat loads for the shaker armature cooling system. A conservative shaker cooling system is essential.

Notice that the Fig. 1 PSD profile has reduced g^2/Hz demand in the 1,500 – 2,000 Hz band where most electrodynamic shakers exhibit armature resonance. This means that the full "resonant boost" from the shaker armature that you can count on with a flat PSD profile is not present when running a shaped PSD profile like Fig. 1. So to make up for this missing boost and to achieve the full 92.4 G rms level as shown, you must use a large KVA Power Amplifier to provide extra shaker drive.

No Band Splitting Needed: Most test labs have to run the Fig. 1 PSD profile as a series of split frequency band tests, due to the limitations of their Shaker and/or Power Amplifier equipment. **Experior runs Fig. 1 as one continuous profile without any band splitting**, using the T2000 Shaker driven by a Power Amplifier rated at 240 KVA output.

The bottom line is this -- for running high g-level, shaped vibration PSD's without band splitting, you need a **large Power Amplifier**, **rugged shaker armature design** and **maximum cooling system performance** for successful testing. That's why Experior uses the T2000 Induct-A-Ring Shaker and companion 240 KVA Power Amplifier to handle these high g rms, shaped PSD profiles.

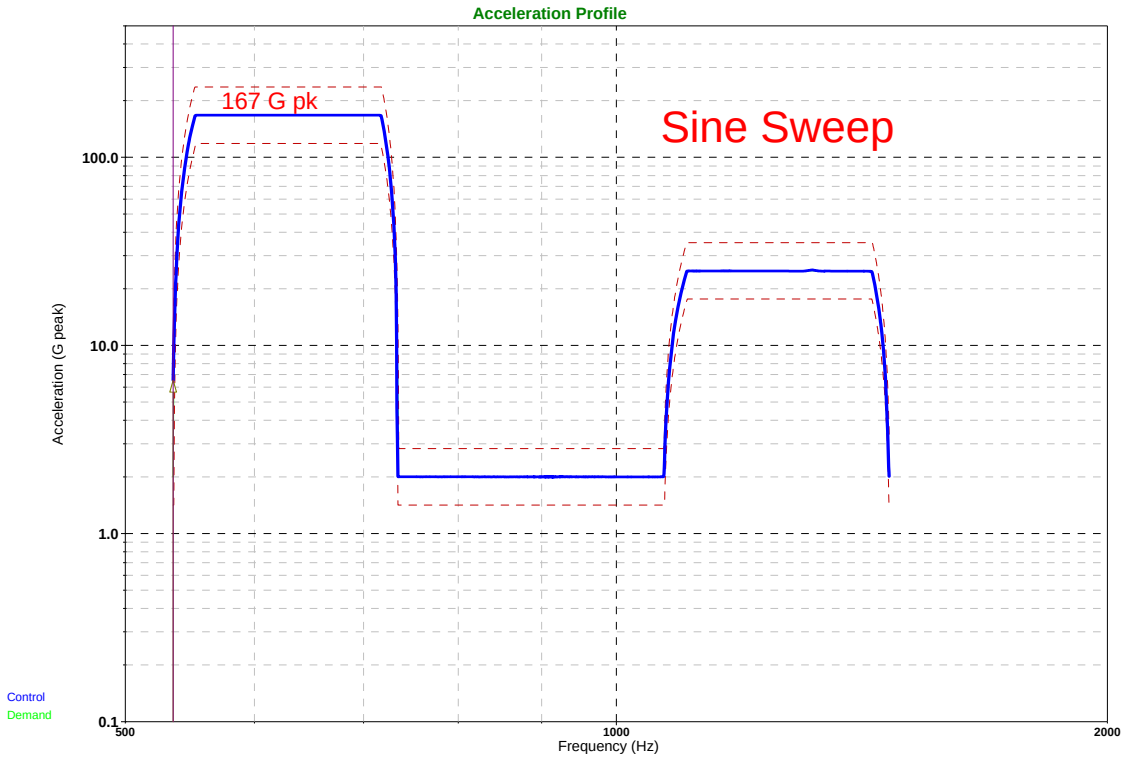


Fig. 2: Sine Sweep Vibration @ 167 g pk (550 Hz – 720 Hz segment)

The test shown in Figure 2 is a demanding sine sweep at g-levels that exceed the max acceleration levels allowed by most electrodynamic shakers. The T2000 Shaker at Experior can deliver this high level sine vibration performance based on the following combination of technical factors:

A. Lightweight Armature: 110 lbs
B. Sine Force Rating: 25,000 lbs pk
C. Solid Metal Induct-A-Ring Armature (no driver coil windings)

This same T2000 Induct-A-Ring Shaker also has excellent low frequency performance, delivering up to **3" pk-pk displacement** which is allows sine testing in the low frequency range required by specifications such as **wind milling vibration**.

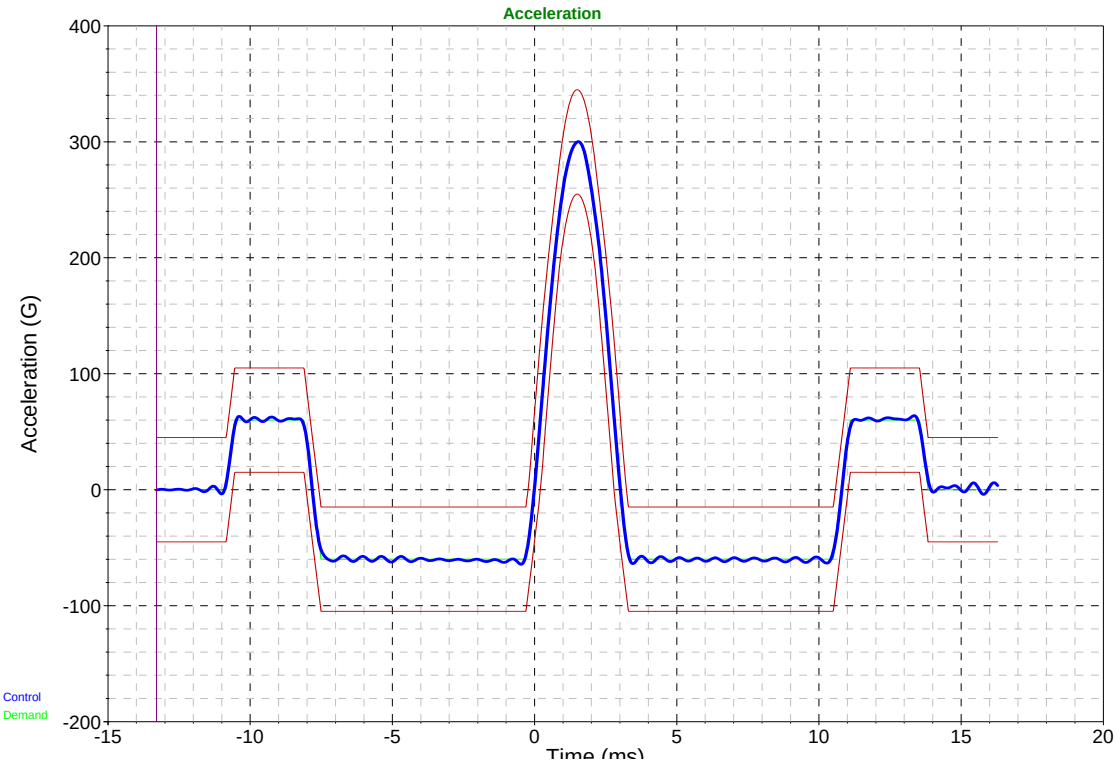


Fig. 3: Classical Shock: 3 msec Half-sine pulse @ 300 g pk

Classical shock pulse test specifications are becoming more demanding as ground vehicle and airborne service environments increase in severity. The 300 g pulse in Figure 3 is required for certain electrical connector test procedures.

Another demanding shock pulse that's often used for qualifying automotive hardware is called out in SAE specs as an 11 msec Half-sine @ 100 g pk. This pulse can be run on an electrodynamic system, if the shaker can produce 2.5" pk-pk stroke and +/- 135 inch/sec pk velocity. These required ratings rule out most of the electrodynamic shakers available at commercial test labs. But the T2000 Shaker at Experior is rated at **3" pk-pk stroke** and **+/- 180 inch/sec velocity**, making the SAE 11 msec @ 100 g shock pulse a routine test.

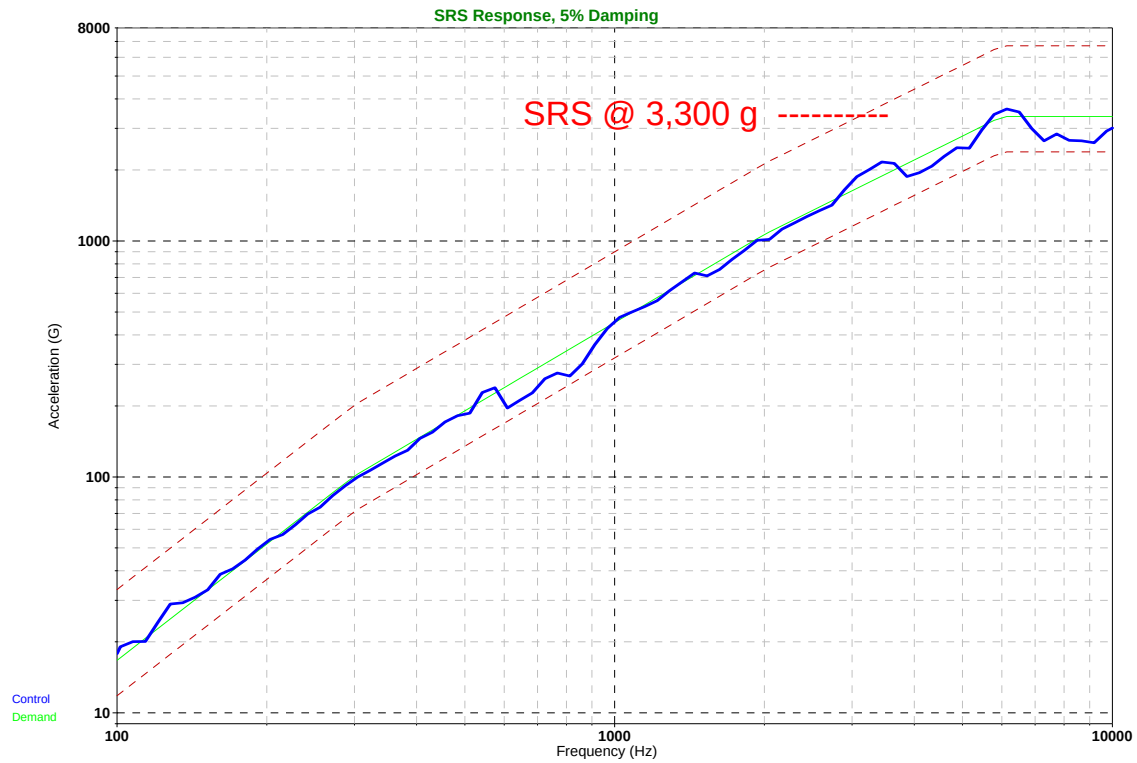


Fig. 4: SRS Shaker Shock @ 3,300 g to 10 KHz (6 KHz Knee Frequency)

Far Field SRS: Until recently, electrodynamic shakers have been limited to the category called "far field" SRS shock -- with a max frequency range of 3,000 Hz.

Far Field SRS tests performed with electrodynamic shakers at most test labs rarely exceed 1,000 g due to Shaker and Power Amplifier limitations.

This historically low ceiling for SRS shaker shock has been dramatically expanded by Experior Labs using its high performance T2000 Shakers. This major breakthrough in SRS shaker shock is linked to the following key factors:

A. T2000 Shaker rated up to 600 g real time armature acceleration (g vs. time)
B. Ultra-High peak current and voltage outputs from the 240 KVA Power Amplifier
C. Addition of a **shock impedance mode** inside the T2000 Shaker to maximize power transfer between the 240 KVA Amplifier and the T2000 Shaker for SRS profiles that demand high drive voltage at the armature input.

With these technical factors in play, SRS levels as high as 5,000 g have been achieved out to 10,000 Hz with lightweight payloads (< 10 lbs), thus substantially exceeding the Far Field SRS limits.

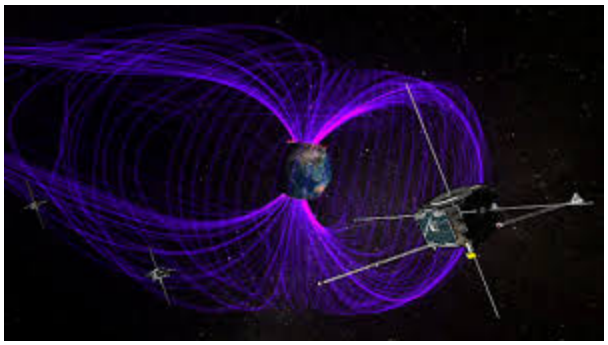
Mid Field SRS: Experior Labs is now in a strong position to deliver SRS testing with its T2000 Shakers for Mid Field SRS pyroshock specifications (out to 10 KHz) at previously unreachable g-levels.

Advantages of SRS Shaker Shock Shaker shock is performed using a PC Controller with accelerometer feedback to lock in the SRS profile as measured at the control accelerometer location. Once the control equalization is completed at low level (typically at -20 dB) the SRS test is brought to full level without overshoot and within relatively tight tolerance bands over the entire frequency range.

The drive spectrum can then be memorized by the Controller so that **all subsequent SRS shocks can be produced with essentially identical profiles.**

About Experior Laboratories

Experior Labs is an independent laboratory that provides environmental testing services for design verification, qualification (QTP) and acceptance (ATP) requirements for hardware manufacturers within the military, aerospace and commercial marketplaces. Experior is located in southern California (Ventura County) and serves a nationwide customer base. Experior specializes in **high g vibration and shock requirements**, and offers competitive pricing with rapid turnaround schedules.



Understanding Single Event Effects For Space Applications

Radiation tolerance is often a key consideration for components and modules in space application designs. This is sometimes secondary to size, weight, power and cost parameters, especially for one-way missions which have no option for repairs or modifications.

Exposure to radiation can cause random, sporadic circuit failures in electronic components which may be temporary or permanent.

The study of radiation on electronic components was begun in the 1950s. As the technology has changed from tubes to solid state, and the transistor sizes have continued to shrink, the potential for adverse effects has increased. This is due to correlations between relative size and charge of the ionizing radiation element to the transistor geometry and the semiconductor substrate thickness.

Ionizing radiation comes in the form of Energetic Protons, Heavy Ions, Alpha Particles, Beta Particles, Galactic Cosmic Rays and others. Neutrons are also included in this classification even though they are not ionizing particles, but their collision with nuclei creates ionizing radiation.

Non-ionizing radiation does not typically have sufficient charge to cause changes to electronic circuitry, and as such is not a concern. This classification includes light (visible and infrared), radio waves, micro-waves and thermal.

One effect of radiation on a semiconductor is that particle strikes create electron-hole pairs in the transistors oxide layer. This causes an increase in the threshold voltage – which requires a higher applied gate voltage to switch a transistor. Another result from charged particle impacts on a transistor is the potential to change the on / off state of the transistor. This can occur when the charge of the particle exceeds that of the transistor element.

Different types of radiation effects, or potential radiation sources, will require varying levels of consideration depending on whether the application is for use at sea-level, atmospheric flight, Earth orbit, extra-terrestrial landing or deep-space exploration.

In all application cases, the effects to the system can be characterized as one or more of the following:

Single Event Effects (SEE) – Soft Errors

- Neutron Single Event Upset (NSEU)
- Single Event Upset (SEU)
- Single Event Transient (SET)
- Single Event Functional Interrupt (SEFI)

Single Event Effects (SEE) – Hard Errors

- Single Event Latch-Up (SEL)
- Single Event Gate Rupture (SEGR)
- Single Event Burnout (SEBR)

Total Ionizing Dose (TID), measured in "rads", is the accumulated exposure of a device to radiation over time. In general, exposure to radiation accelerates the life cycle of a semiconductor, ultimately leading to the failure of the IC .Prior to complete failure, performance parameters decline in an IC as the TID increases over time.

For packaged semiconductor integrated circuits to be certified for space grade applications, they are tested using method-1019 in MIL-STD-883. This destructive testing determines the ability of the component to withstand Total Ionizing Dose (TID) and Enhanced Low Dose Rate Sensitivity (ELDRS). Simply described, this characterizes the components' immunity to SEE based on its threshold to linear energy transfer (LET).

A Cobalt-60 (60Co) gamma ray source is used to generate ionizing particles which travel through the packaged component, and the effects are measured. Standardized testing allows suppliers to create space grade products which can be specified to have a known performance in a space radiation environment.

The complete ~730 page MIL-STD-883 specification is available for download from the Defense Logistics Agency . Radiation effects are generally categorized as either "Soft Errors" or "Hard Errors", and identified as Single Event Effects (SEE). The general category of SEE encompasses all isolated changes to electronic circuitry resulting from interactions with high-energy particles and radiations.
A Soft Error is one which has no long term damaging effects. These can be cleared through normal operation of the device, or in extreme cases through a device reset or power cycle.

Single Event Upset (SEU) is a change in the on / off state of a transistor or a flip in value of a memory bit. Memory errors are routinely checked for, and corrected, using a variety of encoding schemes – the most basic employs one or more parity bits. Rewriting the affected memory location will restore the data to its correct state. Transistors state errors can also be identified using redundancy schemes and major-voting algorithms. The transistor will continue to operate normally and the erroneous state will be

cleared the next time the transistor is toggled. However, a SEU may not be noticed until a particular memory location is read or function of the device is required.

Single Event Functional Interrupt (SEFI) is similar to a SEU in that an upset event changes the state of a transistor, however a SEFI has an immediately noticeable change in the device operation.

Single Event Transient (SET) is more severe type of SEU in which the effect to a single transistor is prorogated to other parts of the circuitry. For example, a SEU in a clock circuit may create errors in all the transistors which are in a particular clock tree or timing domain.

Neutron Single Event Upset (NSEU) events are a subset of SEU which are caused by atmospheric neutron impacts.

Hard Errors typically cause lasting, non-recoverable damage to the circuitry. These cannot be cleared through a system reset or power cycle. Once a hard error occurs, it is permanent.

Single Event Latch-Up (SEL) is also referred to as “stuck bit” phenomena in which a transistor element becomes fixed in either an on or off state, or a memory bit is stuck at either a one or zero. The effected cell is now latched into a permanent state.

Single Event Gate Rupture (SEGR) is a highly destructive impact in which the gate oxide insulation of the transistor absorbs too much energy and ruptures.

Single Event Burnout (SEB) occurs when the Source of a CMOS transistor accumulates additional charge from high energy impacts. The additional charge causes a forward biasing of the transistor. This is of greater concern in power and sensing circuits, rather than logic and control circuits. In a power MOSFET, IGBT or Diode the forward bias can be great enough to cause the circuit to burnout. In extreme cases, the damaged circuit will provide too much current to other transistors and devices, causing a cascading failure.

When designing for space applications, taking into account radiation tolerance and what types of radiation exposures can be expected is critical to meeting the life cycle and performance goals. As semiconductor manufacturing improves, and new technologies such as quantum devices become available, it will become necessary to develop new testing procedures and safeguards.

(Image Credit – NASA)

Hi-Rel Power Management With Peregrine PE9915x Family

Space and Airborne applications usually require ICs which are characterized as High-Reliability ("HiRel" – either as radiation tolerant or radiation hardened) so that the systems can operate properly when subjected to radiation effects. Critical ground systems in Military, Defense and Aerospace may also require similarly rated components.

One subsystem of every design involves powering the components on a PCB. This can be accomplished with a power supply providing all the required voltages for each individual IC, or in many cases with using one or more Point-Of-Load (POL) ICs. With a POL, individual components which have high peak currents, noise susceptibility issues or multiple voltage requirements can have their own dedicated power device. A POL is most often used with high performance ICs such as FPGAs, ASICs and Processors. The switching frequency characteristics can also make POL implementations suitable for many other analog and RF components.

HiRel devices are available from just a few companies, including Peregrine Semiconductor .
Their PE9915x Family of DC-DC Point Of Load (POL) Buck Regulators are run from a standard 5V nominal power supply, and can provide output voltages from 1V to 3.6V. Current output [Iout(max)] can be as high as 10A, depending on the device. Depending on the design requirements, the devices are available as bare die in addition to traditional packaged parts (32-pin CQFP, 12.57 mm x 13.08 mm).
Peregrine specifies these HiRel regulators with radiation-hardness up to 100 KRad (TID / total ionization dose tolerance) and Single Event Effects (SEE) immunity to a Linear Energy Transfer (LET) greater than 90 MeV•cm²/mg. They emphasize their monolithic technology can be used as a replacement to multi-chip modules by offering superior performance, smaller size and reduced weight in sensitive space applications.

The part number selection table and links to data sheets, white papers and additional information is provided below:

Part Number	Iout Max (A)	Vin Min (V)	Vin Max (V)	Vin Typical (V)	Vout Min (V)	Vout Max (V)
PE99151	2	4.6	6	5	1	3.6
PE99151-DIE	2	4.6	6	5	1	3.6
PE99153	6	4.6	6	5	1	3.6
PE99153-DIE	6	4.6	6	5	1	3.6
PE99155	10	4.6	6	5	1	3.6
PE99155-DIE	10	4.6	6	5	1	3.6

(Image Credit - Peregrine Semiconductor)

LTC3612 - Hi-Rel Step Down Converter From Linear Technology

Linear Technology released high reliability (H-grade) and Military (MP-grade) versions of the LTC3612. This is a high efficiency, 4MHz synchronous buck regulator that incorporates a constant frequency, current mode architecture. The device can deliver up to 3A of continuous output current at output voltages as low as 0.6V from a 3mm x 4mm QFN or a thermally enhanced TSSOP-20 package.

The LTC3612 operates from an input voltage of 2.25V to 5.5V, making it ideal for single cell Li-Ion applications as well as 3.3V or 5V intermediate bus systems. Its switching frequency is user programmable from 300kHz to 4MHz, enabling the use of tiny, low cost capacitors and inductors.

The high reliability H grade versions are guaranteed to meet specifications over the -40°C to 150°C operating junction temperature range. The LTC3612HUDC is available in a 3mm x 4mm QFN-20, and the LTC3612HFE is offered in a 20-lead, thermally enhanced TSSOP package.

The military MP grade versions, the LTC3612MPUDC in QFN and LTC3612MPFE in TSSOP, are guaranteed to meet specifications over the -55°C to 150°C operating junction temperature range.

Pricing for the H-grade starts at $3.95 and $4.15 each, respectively in 1,000-piece quantities.

The MP-grade are priced at $9.85 and $10.40 each, respectively in 1,000-piece quantities.

All versions are currently available from stock supplies.

For more information, and links to the data sheet, visit the LTC3612 product page.
(Image Credit - Linear Technology Corporation)

Hi-Rel And High Temperature Electronics Modules Collaboration

M.S. Kennedy and Cissoid Jointly Announce a Long-term Collaboration Agreement for HiRel and High Temperature Electronics Modules. Agreement combines Cissoid's experience in developing semiconductors for extreme temperatures and harsh environments — with M.S. Kennedy's expertise in developing complex, high-reliability multi-chip modules.

Cissoid, the leader in high-temperature and extended lifetime semiconductor solutions, and M.S. Kennedy, a leader in high-temperature and extreme environment modules, jointly announce today they have signed a long-term collaboration agreement to develop high-reliability (HiRel) and high-temperature electronic modules. The agreement brings together Cissoid's 14 years of experience in developing semiconductors that operate in extreme temperatures and harsh environments — with M.S. Kennedy's 43 years of expertise in developing complex high-quality/high-reliability multichip module solutions. Collaboration between the companies will address packaging multiple ICs into new, integrated, and highly compact standard multi-chip module products. Products introduced jointly will address new, high-temperature applications enabling customers to quickly develop their own solutions and reduce time to market.

Cissoid and M.S. Kennedy will shortly announce the details of their first jointly developed standard product based on Cissoid's HADES® V2 — a high-reliability, high voltage, and isolated gate driver solution that will provide a fully integrated solution to its customers. Both companies are also cooperating on custom modules, tailored to specific customer requirements.

“M.S. Kennedy is very excited to be working with Cissoid on developing next generation ultra high temperature products,” said Bill Polinsky, Business Development Manager at M.S. Kennedy. “We see this relationship as key to pushing high-temperature, multi-chip module functionality beyond 232°C.”

Dave Hutton, VP of Worldwide Sales at Cissoid, added that, “Cissoid is very excited about this collaboration. We are working very closely with many market leaders in the oil and gas, aerospace, industrial and automotive markets. As we talk to our customers, we see an increasing requirement for more integrated solutions to address key application areas. The collaboration with M.S. Kennedy will allow us to bring together our combined expertise and excellence into solutions that addresses those market needs.”

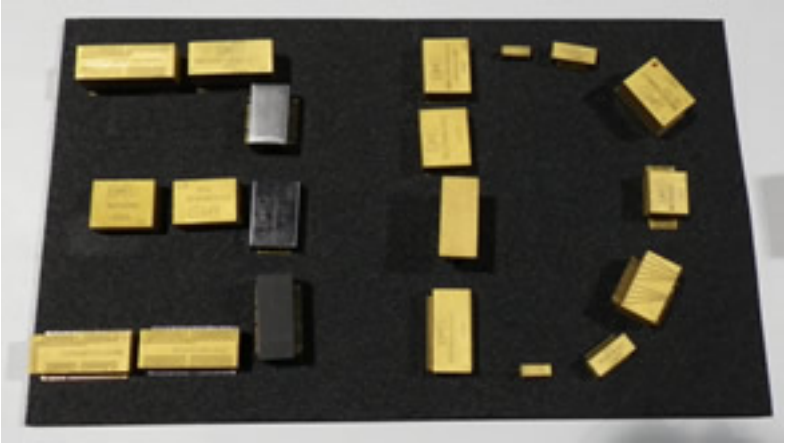
For more information, visit http://www.cissoid.com and http://www.mskennedy.com

About Cissoid

CISSOID is the leader in high temperature semiconductor solutions, delivering standard products and custom solutions for power management, power conversion and signal conditioning in extreme temperature and harsh environments. CISSOID provides high reliability products guaranteed from -55°C to +225°C and commonly used outside that range, from cryogenic lows to upper extremes. Whether the ambient temperature is low but the power dissipation heats up the chips, or in high temperature environments, CISSOID products enable energy, weight and cost savings in lighter, cooling-free and more compact electronic systems. They are used in mission-critical systems as well as in applications requiring long term reliability. CISSOID supplies leaders in the Oil & Gas, Aeronautics, Industrial and Automotive markets.

About M.S. Kennedy

MSK is a leader in the design and production of high performance analog and mixed signal microelectronics. MSK’s standard products include operational and video amplifiers, motor drives and linear regulators – as well as switching voltage regulators. MSK is also a leading producer of custom power modules and multichip modules for Space and Military applications- applying our circuit design expertise and versatile packaging capabilities to each circuit produced. M.S. Kennedy
(Image Credit - M.S. Kennedy)



Space Qualified Standard Products and System In Package Solutions From 3D Plus

It has become increasingly more difficult for developers of Hi-Rel and space level systems to find approved and qualified devices for current and upcoming programs. One company that has flight proven devices for space qualified standard products and system in package solutions is "3D Plus ".

Quality, reliability and size are always critical for any space qualified design, and 3D Plus meets these requirements with a history of more than 55,000 modules in orbit over a period of 13 years of business. 3D Plus has components and modules for a range of applications and industries, including:

- Space
- Aerospace, Aircraft, Avionics
- Defense
- Security
- Industrial
- Medical
- Embedded Systems
- Computing
- Telecom

A summary and background information on 3D Plus, as described on the website:

3D Plus is a world leading supplier of advanced high density 3D microelectronic products and Die and Wafer Level stacking technology meeting the demand for high reliability, high performance and very small size of today's and tomorrow's electronics.

Its patented technology portfolio starts with standard package scale upward to die-size and wafer-level stacking processes, and, enables stacking heterogeneous active, passive, Opto-electronics and MEMS/MOEMS devices in a single highly miniaturized package.

3D Plus offers catalog products upward to more complex System-In-Package (SiP) solutions and associated services.

3D Plus offers high Quality standards:
ISO9001:2008 certification
Manufacturing line and capability domain qualified by the European Space Agency (ESA) and the French Space Agency (CNES) for Space applications
Catalog products listed in the ESA EPPL (European Preferred Parts List) for space applications
Approved supplier for NASA and Jet Propulsion Laboratory (JPL) in the USA
Customers' specific qualifications and approvals

3D Plus is the largest Space qualified catalog products and custom System-In-Packages (SiPs) manufacturer in Europe. Its 3D stacking technology is the sole space qualified worldwide and with a recognized flight heritage of more than 13 years.

Their product portfolio can be represented as "Radiation Tolerant" devices which are suitable for space, avionics and defense application, and "Industrial Grade" devices. The 3D Plus catalog includes:

Products – Radiation Tolerant

- Memory (SRAM, SDRAM, DDR, DDR2, EEPROM, NOR FLASH, NAND FLASH, PROM, MRAM)
- Interfaces (LVDS)
- Point Of Load (POL) Converters (5V input provides a single output voltage adjustable from 1.22V to 4V)
- Peripherals / Protection ICs (Larch-Up current Limiter – LCL)

Products – Other

- Industrial Memory (DDR3, DDR2, DDR1, SDRAM, SRAM, NOR FLASH, NAND FLASH)
- Industrial Solid State Drives – SSD (SLC in 4GB, 8GB, 16GB, 32GB)
- Micro Camera Heads (NTSC and PAL -1/6" and 1/10" CCD)
- System In Packages – SIP (customer specified)

Designers and developers that are looking for radiation tolerant and certified space grade components should start by reviewing the 3D Plus offerings. In addition to all their standard products, they can also provide custom devices, modules and packaging to meet specific OEM needs.

(Image Credit – SourceTech411)

How Kickstarter Is Helping To Promote Private Space Flight

Crowdfunding is helping inventors invent, filmmakers bring their visions to the screen and artists create their own comic books. Yet can this technology-driven approach to funding give a boost to the private space race? A recent story by PCMag boasts a surprising answer: Yes.

First stop: The moon The PCMag story highlights the efforts of Michael Laine, former NASA engineer and the founder of LiftPort. He's trying to develop a new, rocket-less way to get to the moon, what he calls a lunar elevator. Will it work? Who knows? But Laine has attracted the attention of investors through a Kickstarter campaign. His goal for the campaign had been to raise $8,000. Instead, it produced a stunning $110,000.

Why it's needed When NASA ended its space shuttle program, it provided an opening for private entrepreneurs who have the objective of exploring outer space on their own. And that has left an opening, too, for crowdfunding efforts to help provide the money needed for private space exploration.

The power of crowdfunding Planetary Resources has turned to crowdfunding, too, running its own Kickstarter campaign with the goal of raising $1 million to create a low-Earth orbit telescope. As PCMag reports, this campaign has been successful, too. The company in just 32 days received $1.5 million from 17,600 supporters.

Acumor delivers proactive maintenance services through our flat-rate IT Support Service. Designed to reduce your costs, increase your profits and mitigate your business risks, we partner with you as your Virtual CIO and IT Department, allowing you to focus on running your business, not your technology. (Image Credit - Bing Images)